REMARKS

The Applicant thanks the Examiner for the prompt and thorough Office Action dated December 19, 2002.

Applicant has amended the title to the invention as suggested by the Examiner on page 4 of the Office Action.

On page 4 of the Office Action, the Examiner states that the declaration is defective because non-initialed and/or non-dated alterations had been made. In response, Applicant submits a substitute declaration herewith.

Applicant has also amended the claims to obviate the Examiner's objections and rejections, as set forth on pages 4 and 5 of the Office Action.

The Examiner rejected claims 6-25 under 35 U.S.C. §103(a) as being unpatentable over *Usami* in view of *Chan, et al.* Applicant respectfully traverses this rejection in view of the amendment to the claims.

The *Usami* patent discloses a dual damascene method of fabrication of a semiconductor utilizing a mask layer having one or more mask films formed over a silicon dioxide insulation protective film. As shown in FIG. 1F of *Usami*, a trench and via are etched within the metal mask film 15, before transferring the features through the insulation film 4, and underlying dielectric layers 1 and 3. Similarly, in a second embodiment, shown in FIG. 4, the trench and via are etched in the metallic mask films 37 and 35 before being transferred to the underlying dielectrics 21 and 23. In particular, the *Usami* patent discloses a method in which the via is etched first into the metal mask film 15 and a trench is etched into the mask film, after the via is etched.

The *Chan* patent discloses a method for the dual damascene fabrication of an interconnect structure that utilizes a three film (52, 54, 56) mask layer 58. In *Chan*, a trench is first etched into the mask layer 58 without exposing the underlying dielectric. However, *Chan* discloses a method in which the via is etched into the mask layer 58 after etching the trench; however, the via is not etched into the underlying dielectric. That is, the via is etched into the mask layer

58 without exposing the underlying low-k dielectric, before the via and trench features are subsequently etched into the underlying dielectric layers.

In addition, although *Chan* discloses a method by which the via is etched after the trench is etched in the mask layer, the via is etched through the mask layer 58 without exposing the dielectrics 46 and 50, as shown in FIG. 3c. In addition, the top mask film 56 is removed prior to etching the via through the dielectrics 46 and 50, as shown in FIGs. 3f-3i.

Amended claim 6 is distinguishable from *Chan* because the via is etched through the "mask layer and dielectric material to the underlying metal layer before removing remaining portions of the barrier mask film and metallic mask film," *i.e.*, the top two films of the claimed mask layer.

Amended claim 6 also includes forming a barrier film between the passivation film and the metallic mask film, which is not disclosed in *Usami*. Moreover, in amended claim 6, the trench is etched first through the metallic mask film without exposing the underlying low-k dielectric, before the via is etched. Such a procedure may avoid the potential of losing the via feature that may occur in the procedure shown in *Usami*, which discloses etching the via first in the metallic film before etching the trench. With respect to *Usami,* if the trench is over etched, the via may be lost entirely and cannot be transferred to the underlying layer.

Amended claims 6, 13 and 21 are each distinguishable for the above stated reason that a trench is first etched into the mask layer without exposing the underlying dielectric. Then a via is subsequently etched through the mask layer and into the underlying dielectric material.

In view of the foregoing, Applicant respectfully requests reconsideration of the amended independent claims 6, 13 and 21, and claims dependent therefrom.

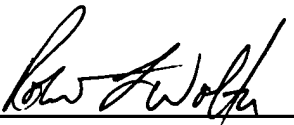
The Applicant's amendments to the claims and/or specific obviate the rejections under 35 U.S.C. §112 with respect to claims 6-20.

Applicant traverses the Examiner's rejection of 24 and 25 under 35 U.S.C. §112 as being indefinite for failing to particularly point out and distinctly claim the subject matter which Applicant regards as the invention. Specifically, the Examiner stated that claims 24 and 25 recite a predetermined width, and that the term "predetermined" rendered the claims indefinite. In addition, the Examiner referred to claim 25 as including the term "predetermined depth." Applicant submits that it is well known in the industry that prior to etching a layer or material on a semiconductor chip, dimensions of a feature that is to be etched are known prior to beginning the etch. The dimension of the feature determines, for example, the length and time of the etching procedure, as well as the etching materials used. Accordingly, one skilled in the art would understand that "predetermined" means that the etching procedure takes place to meet the known and/or desired dimensions of a feature to be etched in a semiconductor chip. "Predetermined" is defined in the *American Heritage Dictionary*, 4th Edition, page 1426 as "a verb to determine, decide or establish in advance."

Applicant respectfully requests the Examiner to reconsider the rejection of the pending claims in view of the foregoing amendments and remarks.

If further prosecution of this application can be facilitated via telephone conference, the Examining Attorney is invited to contact the undersigned at (407) 926-7706.

Respectfully submitted,



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I hereby certify that a true and correct copy of the above and foregoing Amendment was furnished by First Class Mail to the Commissioner of Patents, Box Fee Amendment, Washington, DC 20231, this 18th day of March, 2003.

Gwendolyn Ramsey

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